REMARKS

The claims are claims 1 to 4 and 11 to 14.

Claims 1 to 4 and 11 to 14 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Frankel et al U.S. Patent 4,463,443, Helen et al U.S. Patent 4,616,338 and Nakamura et al U.S. Patent 5,832,308.

Claims 1 and 4 recite subject matter not made obvious by the combination of Frankel et al, Helen et al and Nakamura et al. Claim 1 recites a copy/access controller "operable to prompt said second component to access said second buffer when said data is copied from said first buffer." Claim 11 similarly recites "prompting said second component to access said data in said second buffer when said copying step is completed." These limitations are not made obvious by the combination of Frankel et al, Helen et al and Nakamura et al. The FINAL REJECTION states at the last line of page 3 to page 4, line 5:

> "Frankel fails to explicitly teach the prompting of a second component to access the second buffer when the data is copied from the first buffer. It should be seen that the writing of data to the output shift register is inherently a prompt to the second component to read data out, as writing output data to the register will cause the second component to read data out according to its own second clock signal."

The Applicants submit that the above quoted language of claims 1 and 11 require more than merely writing to the output shift register. This language requires generation of a prompt signal to initiate reading data by the second component. The Applicants submit this limitation is not inherent in the mere writing of data to the buffer. The FINAL REJECTION cites portions of the secondary references Helen et al and Nakamura as making obvious this subject matter.

Helen et al states at column 2, lines 5 to 13 (within the portion cited in the FINAL REJECTION):

> "supplemental means for generating an internal reading request and directing it to said random access memory when said third storing means are in a condition indicating that the first output buffer register is empty and as long as said reading request has not been acknowledged, and for resetting said third storing means into a condition indicating that said first output register is loaded as soon as the reading request has been acknowledged"

This portion of Helen et al states that the reading request from the random access memory is generated "when said third storing means are in a condition indicating that the first output buffer register is empty and as long as said reading request has not been acknowledged." The Applicant respectfully submits that this condition for prompting reading out of the random access memory is neither the condition "when said data is copied from said first buffer" recited in claim 1 nor the condition "when said copying step is completed" recited in claim 11. In particular, the condition triggering the prompt noted in Helen et al is not that recited in claims 1 and 11.

Nakamura et al discloses two uses of the FIFO full signal. Nakamura et al discloses the first use at column 20, lines 49 to 55 (within the portion cited in the FINAL REJECTION):

> "Status 3: FIFO status verification. If the FIFO is not full, the DMA transfer control circuit proceeds to status 4. If it is full, the DMA transfer control circuit remains at status 3. In other words, data is output in this case from the buffer memory (DMA transfer control circuit) to the FIFO, as shown in FIG. 10, but if the FIFO is full, data cannot be input to the FIFO."

This disclosure teaches not transferring data into the FIFO when the FIFO is full. This clearly is a different disclosure than the

above quoted limitation regarding prompting the second component to access the second buffer as recited in claims 1 and 11. This prompt of Nakamura et al does not trigger action in the second component as required by claims 1 and 11. Nakamura et al includes similar teachings at column 22, lines 51 to 53 and at column 26, lines 20 to 23. Nakamura discloses the second use at column 22, lines 1 to 6 (within the portion cited in the FINAL REJECTION):

> "Status 7: If it is determined in status 6 that the FIFO is full, data is transferred from the FIFO to the buffer memory. In other words, after outputting the end imminent signal in status 5, the DMA transfer control circuit waits until the FIFO becomes full (status 6), then transfers data from the FIFO to the buffer memory once it has become full."

This disclosure teaches transferring data from the FIFO into the buffer memory when the FIFO is full. This is not neither prompting a second component to access the second buffer "when said data is copied from said first buffer" recited in claim 1 nor prompting a second component to access the second buffer "when said copying step is completed" recited in claim 11. In order to teach these limitations, Nakamura et al would have to teach prompting reading of the buffer memory under these conditions. Nakamura et al fails to teach this subject matter. Accordingly, claims 1 and 11 are allowable over the combination of Frankel et al, Helen et al and Nakamura et al.

The FINAL REJECTION of October 25, 2005 newly cites description of Status 8 of Nakamura et al at column 22, lines 7 to 16 as anticipating this subject matter. This portion of Nakamura et al states:

> "Status 8: End decision. If the E bit is 1 and the transfer count counter value is 0, it is determined that data transfer has ended, and the DMA transfer control circuit returns to status 1. On the other hand, if the E bit is 0 and

the transfer count counter value is 0, it is determined that the next table data is yet available, and the DMA transfer control circuit returns to status 2 to load the next table data. If the transfer count counter value is not 0, the DMA transfer control circuit returns to status 6 repeats statuses 6 to 8 until the transfer count counter value is 0."

This disclosure of Nakamura et al deals with the end of the DMA transfer. This DMA transfer ends if the E bit is 1, it continues using statuses 6 and 7 if the E bit is 0. Statuses 6 and 7 deal with transferring data from the FIFO to the buffer memory. Nakamura et al teaches neither a prompt to read data from the buffer memory generated by the copy/access controller as recited in claim 1 nor generated as part of the method of claim 11. It is clear from the totality of Nakamura et al that the data in the buffer memory must be read. However, Nakamura et al fails to teach the claimed prompt to read the buffer memory based upon the copy status to the FIFO. The Applicants submit that this limitation recited in claims 1 and 11 is not obvious from the combination of Frankel et al, Helen et al and Nakamura et al.

Claims 2 to 4 and 12 to 14 are allowable by dependence upon respective allowable base claims 1 and 11.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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